What is claimed is:

1. A semiconductor device for refreshing data stored in a memory device, comprising:

a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells;

a tag block having N+1 number of unit tag blocks, each storing at least one physical cell block address denoting a row address storing a data; and

a control means for controlling the tag block and the predetermined cell block table for refreshing the data in the plurality of unit cells coupled to a word line in response to the physical cell block address.

2. The semiconductor device as recited in claim 1, further comprising:

a predetermined cell block table for storing an information representing at least more than one word line among the M number of the word lines storing data.

3. The semiconductor memory device as recited in claim 1, wherein the tag block includes:

an N+1 number of unit tag tables having M number of registers for storing at least one physical cell block address denoting a row address storing a data;

a N+1 number of comparators for checking information

stored in the registers for selecting one word line of the unit cell block with a logical cell block address sensed by the row address;

a encoder for outputting the physical cell block address by encoding results compared by the N+1 number of comparators; and

a tag control block for controlling the N+1 number of the unit tag tables, the N+1 number of the comparators, and the encoder.

4. The semiconductor memory device as recited in claim 3, wherein each register of the unit tag table includes:

a first register having X bits for storing the logical cell block address in response to the N number of unit cell blocks, wherein X is at least $\log_2 N$; and

a second register for sensing an update of data stored in the first register.

5. The semiconductor memory device as recited in claim 3, wherein the tag block further includes:

a decoder for receiving the candidate information and outputting the logical cell block.

6. The semiconductor memory device as recited in claim 2, wherein the predetermined cell block table includes M number of third registers for storing information what unit cell block out of the N+1 number of the physical unit cell blocks

has the M number of the predetermined word lines, each third register having X+1 bits.

7. A method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a tag block having N+1 number of unit tag blocks, each having M number of register for sensing an update of data, comprising the steps of:

(A) starting a refresh mode;

(B) finding at least one physical block address by decoding $(N+1)\times M$ number of second register each storing logical block address; and

(C) performing the refresh operation in the selected unit cell block.

8. The method as recited in claim 7, wherein the step (C) includes the step of

(D) decoding the M number of third registers in the predetermined cell block in order to find out that the M number of predetermined word lines is respectively assigned to which unit cell block among the N+1 number of unit cell blocks,

wherein the refresh operation is performed except for word lines assigned as the M number of the predetermined word line.